

*A1*

the executable programs are loaded from a network connection into the RAM 12 for execution by the microprocessor 10. A Web TV system, which is known in the art, is also considered to be a computer system according to the present invention, but it may lack some of the features shown in FIG. 1, such as certain input or output devices. A typical computer system will usually include at least a processor, memory, and a bus connecting the memory to the processor.

---

Please replace the paragraph starting at line 5 on page 11 with the following:

*A2*

As is conventional, the address space of the video memory is logically divided into several types of buffers, including a frame buffer which is further subdivided into buffers that handle various attributes of a frame, such as color buffer 204. In the present invention, the memory controller 201 logically partitions the address space of the color buffer 204 into a frame-preparation memory 205 and a refresh memory 207. The address space of the frame-preparation memory 205 is mapped to the main memory 203, while the address space of the refresh memory 207 is mapped to a separate, dedicated memory.

---

Please replace the paragraph starting at line 3 on page 12 with the following:

*A3*

Partitioning the memory address space of the color buffer into the frame-preparation memory 205 and the refresh memory 207 decouples the color buffer from main memory by directing the memory traffic necessary to refresh the display device 219 to the separate, dedicated memory instead of to the main memory. The only color data directed to the main memory 203 is for the purpose of forming of a new frame in frame-preparation memory 205 and the extra bandwidth previously required to refresh the display device 219 is now off-loaded to the separate refresh memory 207. This can be an important change since the bandwidth for refresh rate is actually less than the bandwidth for frame formation. Thus, the overall bandwidth requirement of the main memory 203 for graphics operations is reduced by the amount of bandwidth required to sustain the refresh rate of the display device 219.

---